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FIG. 1
(PRIOR ART)

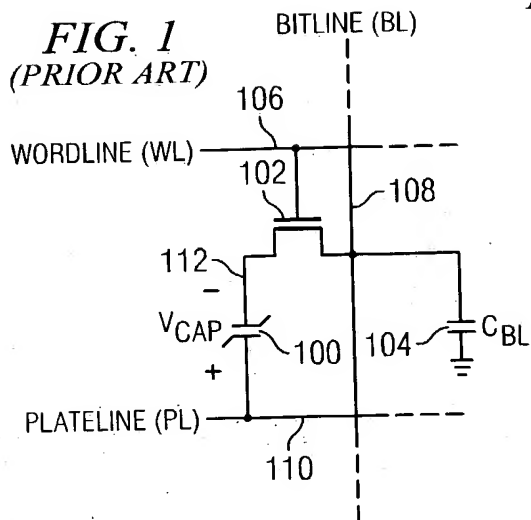


FIG. 2
(PRIOR ART)

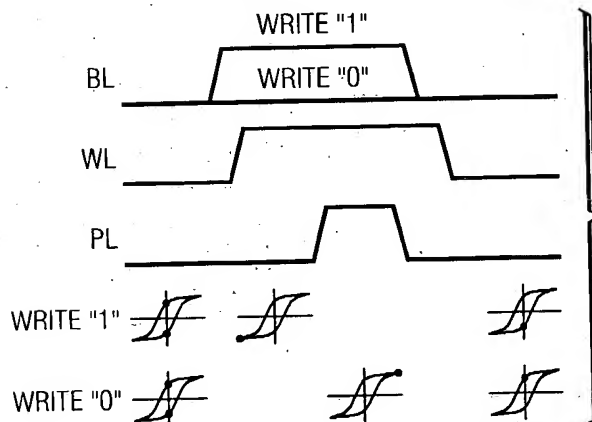
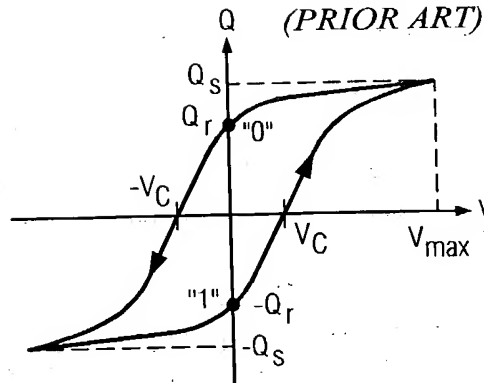


FIG. 3
(PRIOR ART)

FIG. 4
(PRIOR ART)

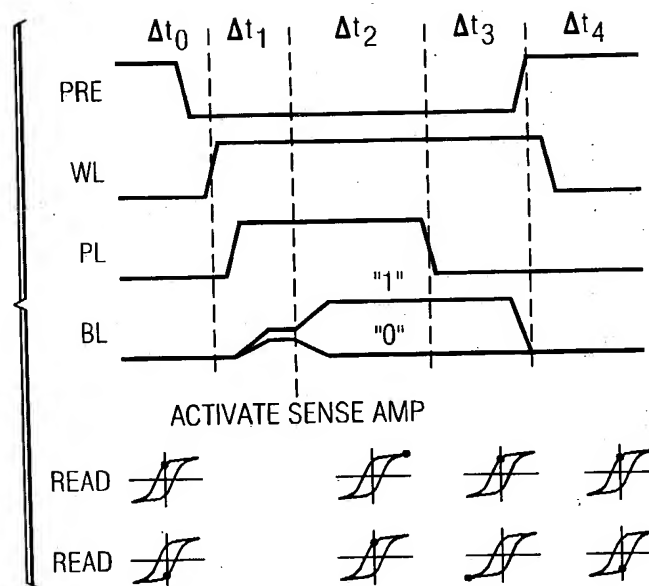


FIG. 5A
(PRIOR ART)

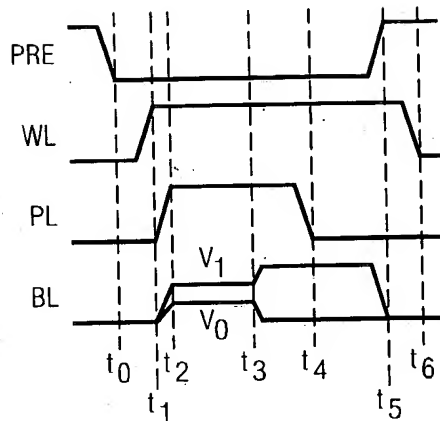


FIG. 5B
(PRIOR ART)

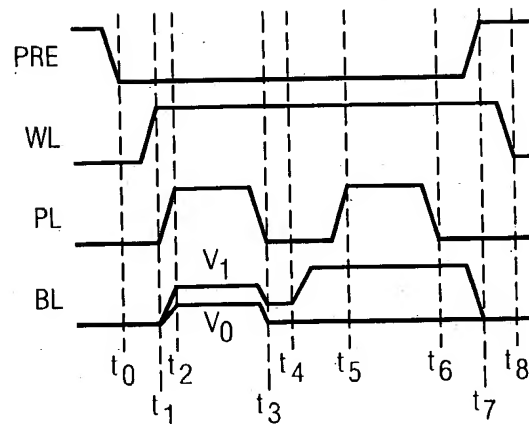


FIG. 6
(PRIOR ART)

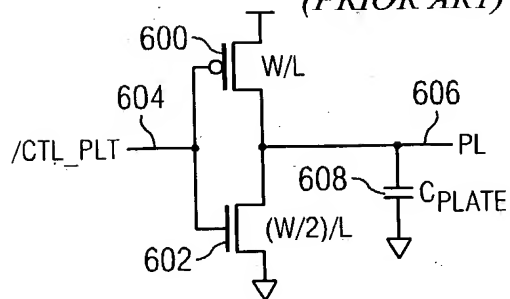


FIG. 7
(PRIOR ART)

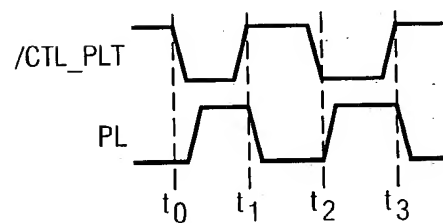


FIG. 8

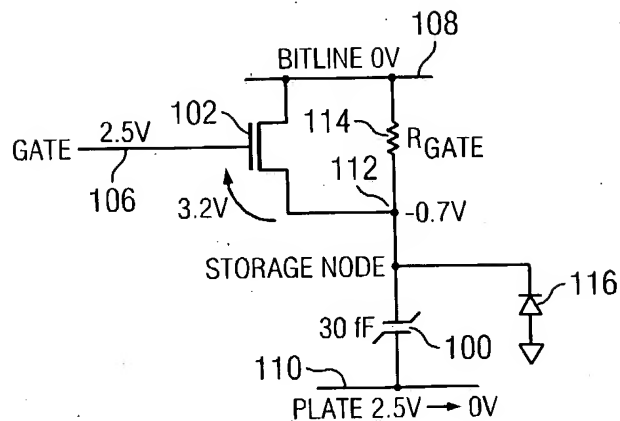


FIG. 10

Timing diagram showing the relationship between the **READ/WRITE** signal, the **/CTL_PLT_RW** signal, and the **PL** signal over time.

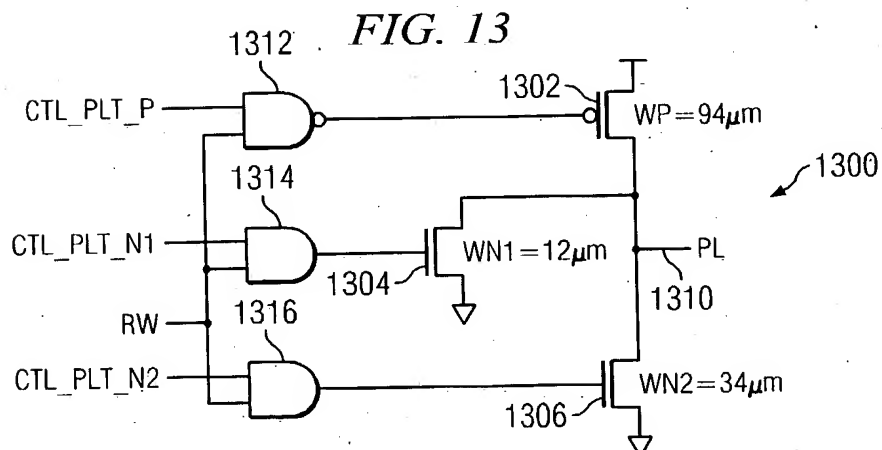
- The **READ/WRITE** signal is high for a read operation and low for a write operation.
- The **/CTL_PLT_RW** signal is active-low, meaning it is low for a read operation and high for a write operation.
- The **PL** signal is the clock signal for the PLD.
- The diagram illustrates the timing constraints for the read and write operations, with specific time points t_0 , t_1 , and t_2 marked on the PL signal.
- Labels **1000** and **1002** point to the rising and falling edges of the PL signal, respectively.

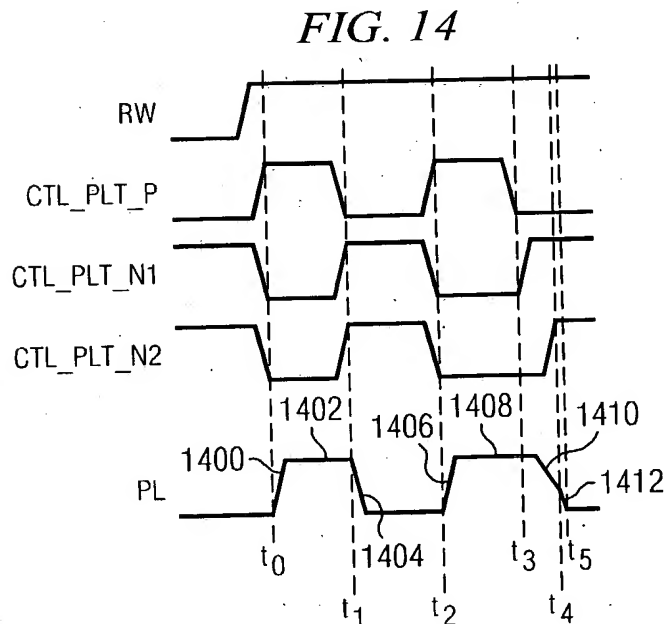
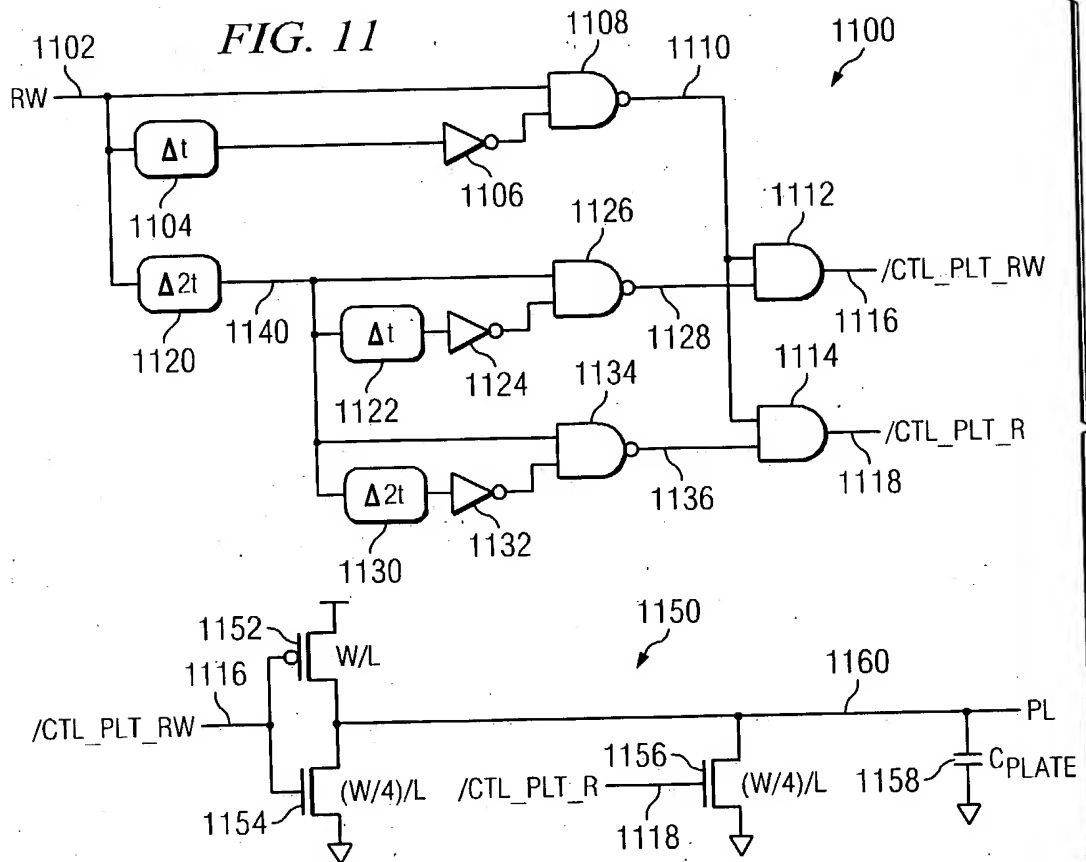
FIG. 12

Timing diagram showing signals RW, /CTL_PLT_RW, /CTL_PLT_R, and PL over time intervals t_0 , t_1 , t_2 , and t_3 . The diagram is divided into READ and WRITE/RESTORE phases.

- RW**: Read/Write signal. High for READ, low for WRITE/RESTORE.
- /CTL_PLT_RW**: Control signal. Low for READ, high for WRITE/RESTORE.
- /CTL_PLT_R**: Control signal. Low for both READ and WRITE/RESTORE.
- PL**: Data signal. High for READ, low for WRITE/RESTORE.

Time intervals t_0 , t_1 , t_2 , and t_3 are marked on the horizontal axis. The signal PL is labeled with 1200 and 1202.





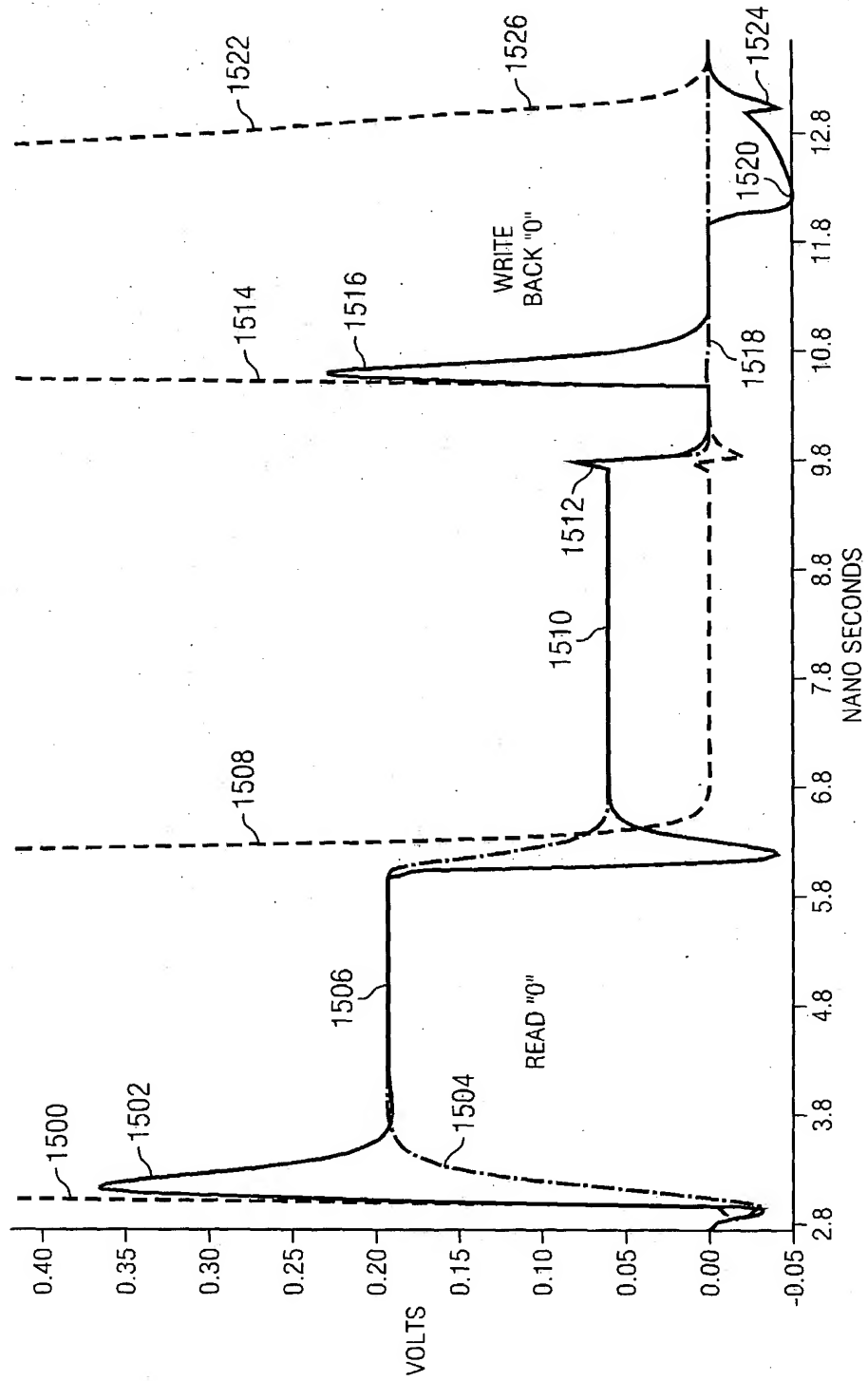


FIG. 15